Jay Sonawane

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Research Interest

Nanoelectronics- Device Physics and Modeling, Characterization and Fabrication

Education

Indian Institute of Technology Bombay   *Jul 2019 – Aug 2024 (expected)*
Electrical Engineering (Dual Degree – B.Tech + M.Tech)
Specialization – Integrated Circuits and Systems, CPI – 8.42

Publications

- **J. Sonawane**, S. Patil, A. Kadam, A. Singh, S. Lashkare, V. Deshpande, U. Ganguly, *"Design Space and Variability Analysis of SOI MOSFET for Ultra-Low Power BTBT Neuron,"* **IEEE Transactions on Electronic Devices (TED)**, under review
  http://arxiv.org/abs/2311.18577
- S. Patil, A. Kadam, **J. Sonawane**, A. Singh, N. Mohapatra, V. Deshpande, and U. Ganguly, *"Reliability of Tunneling Regime for Silicon on Insulator-based Neuron,"* manuscript under preparation
- N. Saurabh*, S Patil*, P Meher, **J. Sonawane**, S. Kumar, B. Kamaliya, S. Lashkare, R. Mote, A. Laha, V. Deshpande, U. Ganguly, *"Structural and Electrical Characterization of Phase Evolution in Epitaxial Gd2O3 due to Anneal Temperature for Silicon on Insulator (SOI) Application,"* Applied Physics Letters (APL), to be submitted

Research Experience

Monolithic 3D Integration (1T-1R): BEOL Indium Tin Oxide MOSFET and HfO2 RRAM   *Aug 2023 – Present*
Dual Degree Thesis, Guide: Prof. Veeresh Deshpande, IIT Bombay

- Modeling dual-gated Indium Tin Oxide channel MOSFET in **Sentaurus TCAD** to be used as a memory access transistor for HfO2 RRAM in the application of monolithic 3D embedded memory integration of 1T-1R resistive RAM cell
- Developed physical model interface **(PMI model)** for **mobility modeling** and demonstrated accurate representation of the SS region of ITO MOSFET incorporating effective interface trap density and ITO bulk donor trap density
- Fabricating back-end of line (BEOL) compatible HfO2 RRAM (Si/W/HfO2/TiO2/W) and ring-gate ITO MOSFET using low-cost **RF sputtering** and **Atomic Layer Deposition** tool enabled with a TCAD-optimized process flow

SOI Device Optimisation for Operation in BTBT Neurons   *May 2022 – Aug 2023*
Supervised Research Exposition, Guide: Prof. Udayan Ganguly, MeLoDe Labs, IIT Bombay
(Received **Undergraduate Research Award (URA01)** in recognition of excellent research)

- Modelled **GF 32nm PD-SOI MOSFET** in **Sentaurus TCAD** for optimization of neuron operating in **band-to-band tunneling** (BTBT) regime to design a **low variability**, **ultra-low power** neuron (compared to ON and SS)
- **Calibrated** the device, characterized trap-assisted and direct **tunneling** regions using Hurkx and NonLocalPath models and created a design space to achieve lower BTBT current, which translates to a **lower spiking frequency**
- Simulated the effect of **variability** caused by random dopant fluctuations **(RDF)**, oxide thickness variation **(OTV)**, and channel-oxide interface traps **(Dit)** and obtained the sensitivity of BTBT, SS, and ON currents to process parameters
- Characterized the GF 32nm PD-SOI MOSFET for voltage and thermal stress using the measure-stress-measure (MSM) method to capture the **reliability** of BTBT regime operation in comparison to SS and ON regimes

Reliability and Variability analysis of SRAM and Sense Amplifier circuits   *May 2023 – Present*
Research Project, Guide: Prof. Souvik Mahapatra

- Incorporated variability-aware degradation at a transistor level for circuit aging through variable Time-0 Vt shifts, specifically for SRAM and sense amplifier circuits with the Circuit Aging Reliability Analysis Tool **(CARAT)**
- Developed a framework using python and HSPICE to analyze and test circuit aging for SRAM and sense amplifier consisting of **noise margin** and **flip time** analysis tests for SRAM and sense delay and voltage tests for sense amplifier
- Scrutinized the analysis of SRAM metrics for data-dependent BTI degradation and process variability

Performance comparison of Patterned SOI over traditional SOI MOSFETs   *Mar 2022 – Present*
Guide: Prof. Udayan Ganguly, MeLoDe Labs, IIT Bombay

- Engineered a novel SOI MOSFET characterized by patterning a **rare earth buried oxide** (Gd2O3) under the channel
- Simulated the structure and created a **Gd2O3 parameter file** necessary to characterize and compare the behavior of traditional and patterned SOI MOSFET in Sentaurus TCAD
- Compared bulk, traditional SOI, and patterned SOI MOSFETs on the basis of performance metrics in ON and SS regimes

Reliability of Cryo-CMOS-based circuits *Aug – Nov 2021*
Summer Undergraduate Research Project (SURP), Guide: Prof. Souvik Mahapatra

- Studied a compact model used to partition the measured threshold voltage shift kinetics for different stresses into **Hot Carrier Degradation**, **Bias Temperature Instability**, and electron/hole trapping subcomponents at low temperature
- Conducted Ngspice simulations for **ring oscillator analysis** to calibrate the compact HCD-BTI model for circuit aging

Skills

Device Fabrication: RF/DC magnetron Sputter, Atomic Layer Deposition, Optical lithography, Annealing furnace
Characterisation: CV and IV measurement (Agilent B1500), Four probe sheet resistance and Hall measurement
Programming: Python, MATLAB, C++, VHDL, Verilog, Assembly, Embedded-C, LaTeX
Softwares: Sentaurus TCAD, HSpice, Cadence Virtuoso, Quartus Prime

Academic Projects

Low SNR input LSM - Optimal Compression and Pre-processing *Oct – Nov 2022*
Course: EE746 Neuromorphic Engineering – Instructor: Prof. Udayan Ganguly

- Modeled a **liquid state machine** (LSM) and simulated pre-processing chain based on **Lyon's Auditory Cochlear** model
- Improvised the pre-processing chain, LSM reservoir, and output classification set of neurons to train the network for low SNR input (10dB) by achieving **similar spiking response** as compared to high SNR input (52dB)

Resonant Tunneling Diodes: NEGF-Poisson based consistent simulation *Mar – Apr 2023*
Course: EE755 Quantum Transport in Nanoscale Devices – Instructor: Prof. Bhaskaran Murlidharan

- Simulated tunneling probability using the **Breit-Wigner function** for varying quantum well and barrier parameters
- Modelled a resonant tunneling diode heterostructure using a self-consistent **NEGF-Poisson formulation** in MATLAB to study the impact of variation in quantum well and barrier parameters on transmission coefficient and I-V characteristics

Serializer-Desierializer Design *Mar – Apr 2023*
Course: EE800 High-Speed Interconnects – Instructor: Prof. Shalabh Gupta

- Designed a 10:1 de-serializer and a 1:10 serializer in **Cadence** and verified using a 10 Gbps signal from a PRSB source
- Designed a half-range **bang-bang phase detector** using 0 and 90-degree clocks to generate the 10 Gbps PRBS signal

Modified WKB-based analytic model for direct tunneling current in MOS devices *Mar – Apr 2022*
Course: EE620 Physics of Transistors – Instructor: Prof. Souvik Mahapatra

- Studied the modeling of direct tunneling current in MOS devices as a function of oxide field and field dependencies
- Reproduced the results using a modified WKB approach consisting of the usual WKB tunneling probability valid for smoothly varying potentials and a reflection coefficient for **correcting reflections** from potential discontinuities

Cascode CS-LNA Design *Mar – Apr 2022*
Course: EE619 RF Microelectronics – Instructor: Prof. Jayanta Mukherjee

- Designed a single-ended **cascoded common source** Low Noise Amplifier (CS-LNA) in UMC 180nm CMOS technology
- Achieved a **noise figure (NF)** less than 2 dB and forward voltage gain greater than 15 dB for operation in **23.5-24GHz**
- Designed the amplifier to have IIP3 greater than -8dB and input-output port voltage reflection coefficients < -10dB

Operational Transconductance Amplifier with Class-B Slew Rate Boosting *Oct – Nov 2021*
Course: EE618 CMOS Analog VLSI Design – Instructor: Prof. Maryam S. Baghini

- Designed an operational transconductance amplifier with slew rate boosting (> **900** μVs) in PTM 130nm technology
- Engineered the amplifier to have a DC gain greater than **70dB** with a gain bandwidth product greater than **1GHz**
- Achieved the total static power consumption of Class B and the main pseudo class AB amplifier less than **4.25mW**

Improving Photoluminescence in InAs Surface Quantum Dots *Mar – Apr 2021*
Course: EE728 Growth and Characterization of Nanoelectronic Materials – Instructor: Prof. S. Chakrabarti

- Simulated InAs SQDs in NextNano ++ software to observe the effects of **extended planar growth** and dot formation
- Scrutinized the effect of antimony (Sb) to delay three-dimensional (3D) growth in InAs surface quantum dots to render **improvement in carrier confinement**, lower energy band gap, and **achieve longer emission wavelength**

20 MHz Transimpedance Amplifier (TIA) for POF applications *Mar – Apr 2022*
Course: EE344 Electronic Design Lab – Instructor: Prof. Joseph John

- Designed a 3-stage closed-loop transimpedance amplifier using CS JFET and 2 CE BJTs with collector-base biasing
- Engineered **low noise, high gain** amplifier featured with 20MHz of bandwidth for plastic optical fiber communication
- Tested the circuit on PCB, transmitted and received a pseudorandom binary sequence using an LED and PIN photodiode

Industrial Experience

Atomberg Technologies   *May – Jul 2022*
Research and Development Intern – Mentor: Gaurav Gupta, Yash Sanghvi   *Pune, India*

- Integrated **PIR (pyro-electric IR)** sensors with **BLDC** smart fans for motion/presence detection-based operation
- Tested and integrated Panasonic and Holtek PIR sensor modules on **STM8s** in Renesa fans and **esp32c3**-based fans
- Developed firmware register transfer level (RTL) code for the GV4 and GV5 series of boards and tested the installation

Carnot Technologies   *May – Jul 2021*
Data Science Intern – Mentor: Yash Sanghvi   *Mumbai (Work from Home)*

- Programmed a script that provides **time series NDVI** files using **Sentinel-hub API** and latitude-longitude boundary
- Statistically analyzed sugarcane crop **NDVI** progression for around **200+** farms around the country for one crop cycle
- Developed a model using a **Random Forest** regressor to predict sugar content in crops using ten **vegetation indices**

Academic Achievements

2023: Received **Undergraduate Research Award (URA01)** for excellent contribution to research
2019: Achieved **All India Rank 1446** in Joint Entrance Exam-Main out of 0.94 million candidates
2019: Secured **All India Rank 2487** in Joint Entrance Exam-Advanced out of 0.25 million candidates

Specialisation Courses

Nanoelectronics	Neuromorphic Engineering
Quantum Transport in Nanoscale Devices	CMOS Analog VLSI Design
Physics of Nanoscale Devices - I	VLSI Design (Theory and Lab)
Physics of Transistors	Radio Frequency Microelectronics Chip Design
Growth and Characterization of Nanoelectronic Materials	High Speed Interconnects: Signaling and Synchronization
Microelectronics Technology Lab	Algorithmic Design of Digital Systems

Teaching and Mentorship Experience

Teaching Assistant, Neuromorphic Engineering   *Jul 2023 – Nov 2023*
Department of Electrical Engineering, IIT Bombay

- Mentoring **130+ participants** for the course, helping them overcome hurdles through doubt clearing and tutorials
- Involved in the **evaluation of examinations**, assessments, and projects conducted during the duration of the course

Department Academic Mentor, Electrical Engineering   *Jun 2022 – May 2023*
Student Mentorship Program, IIT Bombay

- Part of a 40-membered team, selected from **100+ applicants** on the basis of interviews and extensive peer review
- Mentoring twelve sophomores to help them with academic issues, time management, and extracurricular endeavors

Convener, Institute Technical Council   *Jun 2020 – Apr 2021*
Electronics and Robotics Club, IIT Bombay

- A **core member** of a **fifteen-member** group aimed to organize 20+ events, competitions, and hackathons
- Conducted a fully virtual Club Orientation program and a two-day **Arduino boot camp** addressing about 200 freshmen

Extracurricular Activities

Hobbies: Dance, table tennis, badminton, e-sports (Valorant)
2022: Member of the Hip Hop dance team in the Annual Insync Dance Show (AIDS)
2020: Represented IIT Bombay in UMANG, an inter-college dance competition in solo dance
2020: Completed year-long training in Table Tennis under the National Sports Organisation, IIT Bombay
2019: Finalist in the Freshiezza solo dance competition organized by Insync, IIT Bombay for freshmen
2012: Qualified the first four professional tabla exams conducted by the ABGMV Mandal, Mumbai

References

Prof. Udayan Ganguly	**Prof. Veeresh Deshpande**	**Prof. Souvik Mahapatra**
Electrical Engineering, IIT Bombay, udayan@iitb.ac.in	Electrical Engineering, IIT Bombay, veeresh@iitb.ac.in	Electrical Engineering, IIT Bombay, souvik@ee.iitb.ac.in