Jay Sonawane

PH.D. STUDENT · ELECTRICAL AND COMPUTER ENGINEERING

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Education

Georgia Institute of Technology — *Atlanta, U.S.A.*

PH.D. *Electrical and Computer Engineering* — *Aug 2024 - Present*

BEOL and ferroelectric devices characterization and modeling

- Advisor: Prof Shimeng Yu

Indian Institute of Technology Bombay — *Mumbai, India*

DUAL DEGREE PROGRAM: *B.Tech, M.Tech Electrical Engineering* — *Jul 2019 - Jun 2024*

Specialization: Nanoelectronics and Integrated Circuits

- Awarded **Undergraduate Research Award 01 (URA01)** and the **Undergraduate Research Award (Experimental)** for exceptional undergraduate research work
- Advisors: Prof Veeresh Deshpande, Prof. Udayan Ganguly and Prof. Souvik Mahapatra

Research Interests

Advanced Logic Monolithic and Heterogeneous 3D Integration, Device and Circuit Reliability, Variability

Emerging Memories In-memory computing, Non-volatile Memories, Neuromorphic Computing

Publications

1. **J. Sonawane**, P. Chatterjee, and S. Mahapatra, **"Activity Compatible Device-to-Circuit Framework for Process, BTI and HCD Variability"**, International Integrated Reliability Workshop 2024 (IEEE IIRW 2024)
2. **J. Sonawane**, S. Patil, A. Kadam, A. Singh, S. Lashkare, V. Deshpande, U. Ganguly, **"Design Space and Variability Analysis of SOI MOSFET for Ultra-Low Power BTBT Neuron"**, IEEE Transactions on Electronic Devices (IEEE TED) [**Paper**]
3. S. Patil, A. Kadam, R. Saikia, **J. Sonawane**, K. Thakor, A. Singh, Guarav R., N. Mohapatra, V. Deshpande, L. Somappa and U. Ganguly, **"Reliability of Tunneling Regime for Silicon on Insulator-based Neuron"**, IEEE Transactions on Electronic Devices (IEEE TED) [**Paper**]
4. S. Patil, A. Kadam, **J. Sonawane**, A. Singh, N. Mohapatra, V. Deshpande, and U. Ganguly, **"Area and Energy Efficient Quantum Tunneling based Thermal Sensor on 45nm RFSOI Technology,"** IEEE Transactions on Electronic Devices (IEEE TED) [**Paper**]
5. S. Patil, A. Kadam, **J. Sonawane**, S. Deshmukh, S. Lashkare, V. Deshpande, and U. Ganguly, **"Bulk-Silicon based Band-to-band tunneling Neuron"**, IEEE Transactions on Electronic Devices (IEEE TED), under review

Research Experience

BEOL and FeFET devices Modeling and Characterization | PhD Thesis — *Georgia, United States*

Guide: Prof. Shimeng Yu, Laboratory of Emerging Devices and Circuits, Georgia Tech — *Aug '24 - Present*

BEOL Indium Tin Oxide FET for Monolithic 3D Integration | Master's Thesis — *Mumbai, India*

Guide: Prof. Veeresh Deshpande, Oxi-Chan Group, MeLoDe Labs — *Aug '23 - Jun '24*

- Fabricated Indium Tin Oxide transistor as memory access using a back-end of the line (BEOL) compatible process flow
- Achieved low-leakage ITO Back-gate FETs with an ON current of 2 µA/µm and OFF current of 1.2 pA/µm in 10 µm device
- Modeled Indium Tin Oxide channel transistor in Sentaurus TCAD, developed a mobility physical model interface for post threshold (ON) operation and ITO bulk, interface traps for sub-threshold operation

Device Optimization for Band-to-Band Tunneling Neurons | IIT Bombay *Mumbai, India*

Guide: Prof. Udayan Ganguly, MeLoDe Lab | Head: SemiX, IITB *May '22 - Aug'23*

- Modeled GF 32nm PD-SOI MOSFET in Sentaurus TCAD for optimization of low variability, low power BTBT neuron
- Characterized trap-assisted and direct tunneling regions using Hurkx and NonLocalPath models and created a design space to achieve lower BTBT current, translating to a lower spiking frequency akin to biological neurons
- Performed variability study due to random dopant fluctuations, oxide thickness variation, and interface traps to obtain the sensitivity of BTBT, SS, and ON currents to process parameters and tested the reliability in BTBT regime

Activity Compatible Device-to-Circuit Reliability Framework | IIT Bombay *Mumbai, India*

Guide: Prof. Souvik Mahapatra, IIT Bombay *Jul '23 - Jun '24*

- Developed a simulation framework (CARAT) to analyze FET-level process, BTI, and HCD variability impacts on circuits
- Simulated circuit-level BTI and HCI variability for large and small circuits influenced by realistic input gate excitations

Technical Skills

Device Fabrication and Characterization	RF/DC magnetron Sputter, Atomic Layer Deposition, Optical lithography, Annealing furnace, CV and IV measurement (Agilent B1500), Four probe sheet resistance and Hall measurement
Languages and Softwares	Python, MATLAB, C++, VHDL, Verilog, Assembly, Embedded-C, LaTeX, Sentaurus TCAD, HSpice, Cadence Virtuoso

Professional Experience

Atomberg Technologies | Research and Development Intern *Pune, India*

Mentor: Gaurav Gupta, Yash Sanghvi *May – Jul 2022*

- Integrated PIR (pyro-electric IR) sensors with BLDC smart fans for presence/motion detection-based efficient operation
- Tested and integrated Panasonic and Holtek PIR sensor modules on STM8s in Renesa fans and esp32c3-based fans
- Developed firmware register transfer level (RTL) code for the GV4 and GV5 series of boards and tested the installation

Carnot Technologies | Data Science Intern *Work From Home, India*

Mentor: Yash Sanghvi *May – Jul 2021*

- Programmed a script that provides time series NDVI files using Sentinel-hub API and latitude-longitude boundary
- Statistically analyzed sugarcane crop NDVI progression for around 200+ farms around the country for one crop cycle
- Developed a model using a Random Forest regressor to predict sugar content in crops using ten vegetation indices

Key Projects

Low SNR Input LSM - Optimal Compression and Pre-processing

Course: Neuromorphic Engineering – Instructor: Prof. Udayan Ganguly *Oct '22 - Nov '22*

- Modeled a liquid state machine (LSM) and simulated pre-processing chain based on Lyon's Auditory Cochlear model
- Improvised the pre-processing chain, LSM reservoir, and output neurons to train the network for low SNR input (10dB)

Resonant Tunneling Diodes: NEGF-Poisson based consistent simulation

Course: Quantum Transport in Nanoscale Devices – Instructor: Prof. Bhaskaran Murlidharan *Mar '23 - Apr '23*

- Simulated tunneling probability using the Breit-Wigner function for varying quantum well and barrier parameters
- Modeled a resonant tunneling diode heterostructure using a self-consistent NEGF-Poisson formulation in MATLAB to study the impact of quantum well and barrier parameters on transmission coefficient and I-V characteristics

Performance comparison of Patterned SOI over traditional SOI MOSFETs

Course: Nanoelectronics – Instructor: Prof. Udayan Ganguly *Mar '22 - Apr '22*

- Simulated and designed a novel patterned, U gate SOI MOSFET with Gd2O3 as buried oxide in Sentaurus TCAD
- Compared performance metrics of bulk, traditional SOI, and patterned SOI MOSFETs in ON and SS regimes

Serializer-Deserializer Design

Course: High-Speed Interconnects – Instructor: Prof. Shalabh Gupta *Mar '23 - Apr '23*

- Designed a 10:1 deserializer and a 1:10 serializer in Cadence and verified using a 10 Gbps signal from a PRSB source
- Designed a half-range bang-bang phase detector using 0 and 90-degree clocks to generate the 10 Gbps PRBS signal

Modified WKB-based Analytic Model for Direct Tunneling Current in MOS Devices

Course: Physics of Transistors – Instructor: Prof. Souvik Mahapatra *Mar '22 - Apr '22*

- Studied the modeling of direct tunneling current in MOS devices as a function of oxide field and field dependencies
- Reproduced results using a modified WKB approach, correcting reflections from potential discontinuities

Cascode CS-LNA Design

Course: RF Microelectronics – Instructor: Prof. Jayanta Mukherjee *Mar '22 - Apr '22*

- Designed a single-ended cascoded common source Low Noise Amplifier (CS-LNA) in UMC 180nm CMOS technology
- Achieved a noise figure (NF) less than 2 dB and a forward voltage gain greater than 15 dB for operation in 23.5-24GHz
- Designed the amplifier to have IIP3 greater than -8dB and input-output port voltage reflection coefficients < -10dB

Operational Transconductance Amplifier with Class-B Slew Rate Boosting

Course: CMOS Analog VLSI Design – Instructor: Prof. Maryam S. Baghini *Oct '21 - Nov '21*

- Designed an operational transconductance amplifier with slew rate boosting (> 900 μVs) in PTM 130nm technology
- Engineered the amplifier to have a DC gain greater than 70dB with a gain bandwidth product greater than 1GHz
- Achieved total static power consumption of Class B and the main pseudo-class AB amplifier less than 4.25mW

Improving Photoluminescence in InAs Surface Quantum Dots

Course: Growth & Characterization of Nanoelectronic Materials – Instructor: Prof. Chakrabarti *Mar '21 - Apr '21*

- Simulated InAs SQDs in NextNano++ software to observe the effects of extended planar growth and dot formation
- Analyzed the impact of antimony (Sb) to delay 3D growth in InAs surface quantum dots, resulting in improved carrier confinement, lower energy bandgap, and longer emission wavelength

20 MHz Transimpedance Amplifier (TIA) for POF Applications

Course: Electronic Design Lab – Instructor: Prof. Joseph John *Mar '22 - Apr '22*

- Designed a 3-stage closed-loop transimpedance amplifier using CS JFET and 2 CE BJTs with collector-base biasing
- Engineered a low noise, high gain amplifier featuring 20MHz of bandwidth for plastic optical fiber communication

Teaching & Mentorship Experience

Autumn 2023-24	EE 746: **Neuromorphic Engineering**, *Graduate-level course*
Spring 2023-24	EE 724: **Nanoelectronics**, *Graduate-level course*
2022-23	DAMP: **Department Academic Mentor**, *Academic mentor to College Sophomores*
2020-21	Convener: **Electronics & Robotics Club**, *Institute Technical Council*

Key Courses Undertaken

Integrated Circuits	Microelectronic System Packaging, Neuromorphic Engineering, CMOS Analog VLSI Design, Digital VLSI Design (Theory and Lab), Radio Frequency Microelectronics Chip Design, High Speed Interconnects: Signaling and Synchronization, Algorithmic Design of Digital Systems
Solid State Physics	Introduction to Microelectronics Technology, Nanoelectronics, Quantum Transport in Nanoscale Devices, Physics of Nanoscale Devices, Physics of Transistors, Growth and Characterization of Nanoelectronic Materials, Microelectronics Technology Lab
Maths	Calculus, Linear Algebra, Probability and Random Processes, Differential Equations, Machine Learning